WHITE PAPER

Customizing Processes for Hermetic Assembly Of Devices Designed for Plastic Packages

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Abstract

Today's leading-edge semiconductor devices are designed and manufactured for high volume, low cost industrial and consumer based products. The design and layout of these new integrated circuits (ICs) favor plastic molded assembly with an eye toward reduced cost, not dependability. This leaves the high reliability, low volume military and aerospace applications with fewer hermetic package choices directly from the Original Component Manufacturer (OCM). The challenge exists to bridge the reliability requirements of military and aerospace communities with leading edge ICs designed for the mass market.

Introduction

The demands of the commercial and industrial markets have driven the semiconductor industry towards miniaturization, increased yield to maximize productivity, and reduce cost. This drive for cost reduction pushes the boundaries of minimizing die size, bond pad size, and pitch. Process Control Monitors (PCMs) were found traditionally in each reticle. PCM has now moved to the scribe lines to maximize useable space for die fabrication (Figure 1.1).

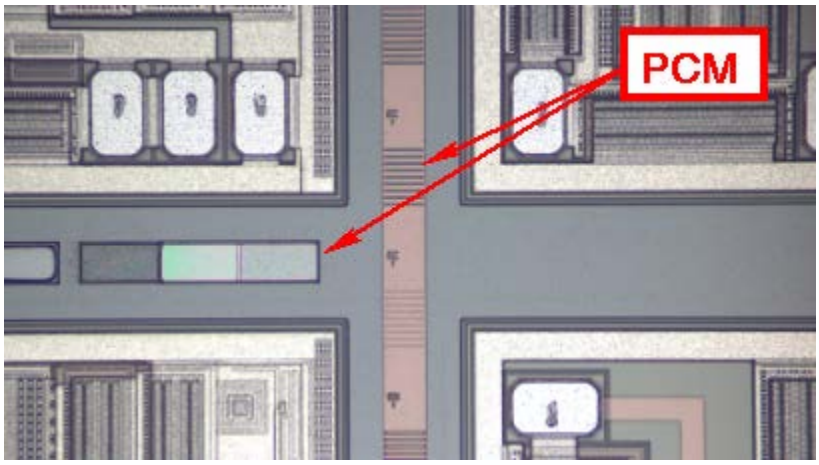


Figure 1.1: Typical PCM Location before saw

First Assembly Process Modification: Wafer Saw Experiment

The need to remove the PCM from the scribe lines can cause assembly issues with high-reliability hermetic IC packages. Hermetic packages have air cavities so loose Foreign Object Debris (FOD) generated from the wafer dicing process of the PCM can cause both optical inspection rejects (per MIL-STD-883 TM2010) and electrical failures in the field. Conductive metal from the PCM, if later dislodged, could short between bond wires, bond pads or any circuitry opening on the die surface (See Figure 1.2).

This issue does not exist in the Plastic Encapsulated Microcircuits (PEMs) as the entire die and internal package leads are encased in plastic which will trap any FOD.

Several ways exist for removing the PCM from the scribe line. One method uses a narrow saw blade (under half the scribe line width) with two shallow sawing passes and a final complete saw. The shallow cut depth is enough to remove the surface metallization of the PCM. The final step is a complete cut through the entire depth of the wafer at the middle of the scribe line. This process employs a single blade allowing the use of the same saw station without any blade changes or removal of the wafer from the saw equipment.

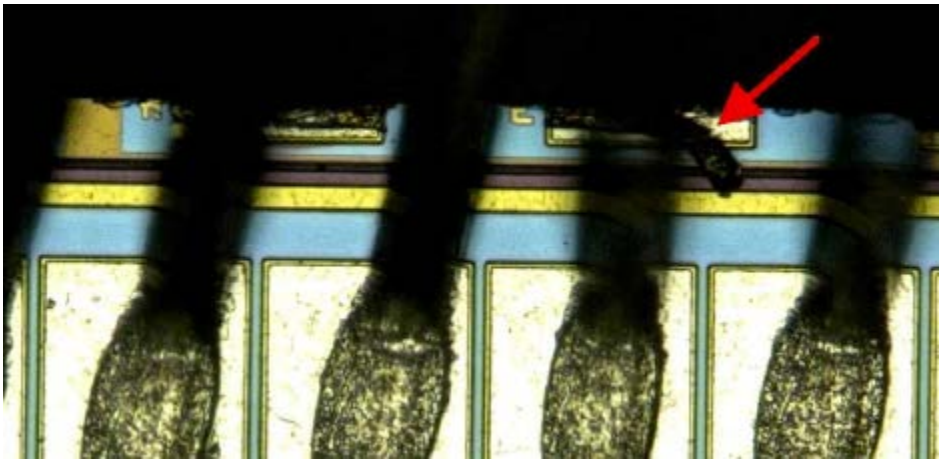


Figure 1.2: Residual metal from PCM

A variation on this method calls for the removal of the PCM with a saw blade as wide as the PCM and at a cut depth just below the PCM metallization. The final cut uses a standard saw blade with exposure greater than the wafer thickness and a blade width under half of the scribe line width. This method requires the use of two different saw stations. The wafer must be removed from the wider blade station and mounted on the saw station with a thinner blade.

An alternative method uses a saw blade just as wide as the PCM metallization and cuts in a single pass. This method saves time as it's just a single cut. Drawbacks to this process include the need to slow down the saw cut speed and constant monitoring of the cut to avoid any blade wobble or equipment drift.

In this particular example, a 2830 blade was used (see Figure 1.3). This blade selection matches the PCM metallization on this particular step pattern. The PCM is 2.65 mil wide, so 2.8 mil wide blade will completely remove all PCM metallization.

Figure 1.3: Top view of alternative method

Issues With PCM Removal

Figure 1.4 shows an example of blade wobble using a 3030 blade. While not a concern for commercial grade part, this chipping will not pass muster in the high-reliability world. In this example, the initial blade selected for PCM removal was much wider than the PCM. Reduction of the saw cut speed can help decrease blade wobble, but with other trade-offs. Reducing the blade thickness from 3 mils to 2.8 mils adds another level of security as there is now additional room for error.

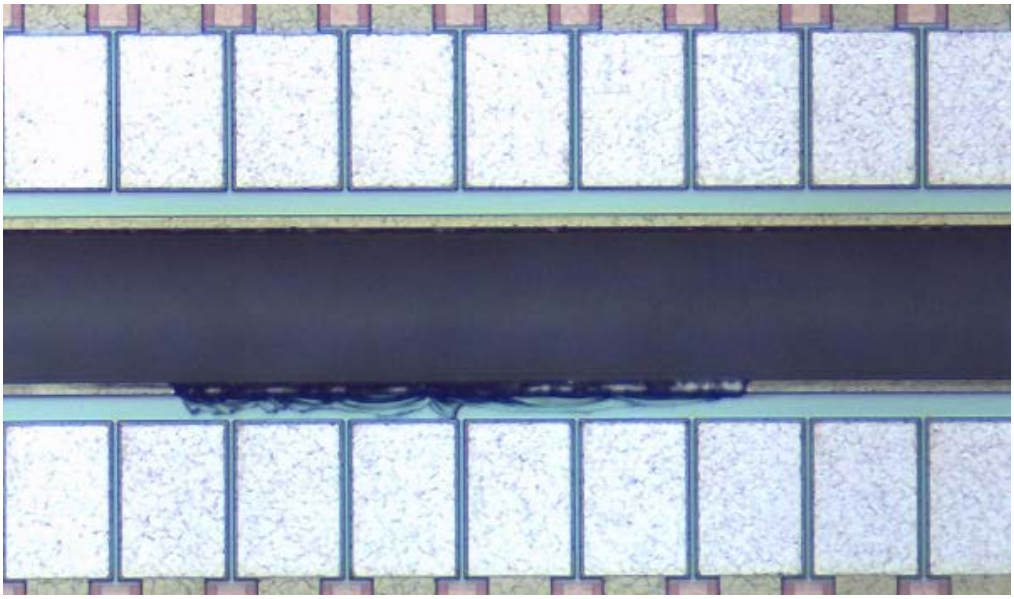


Figure 1.4: Blade wobble developed using 3030 blade at normal cut speed.

Wafer Saw Results

Eliminating the saw street PCM with the use of blades wider than the PCM works, but the drawbacks include longer processing time (slow table speed) and increased silicon dust on the exposed bonding pads (see Figure 1.5).

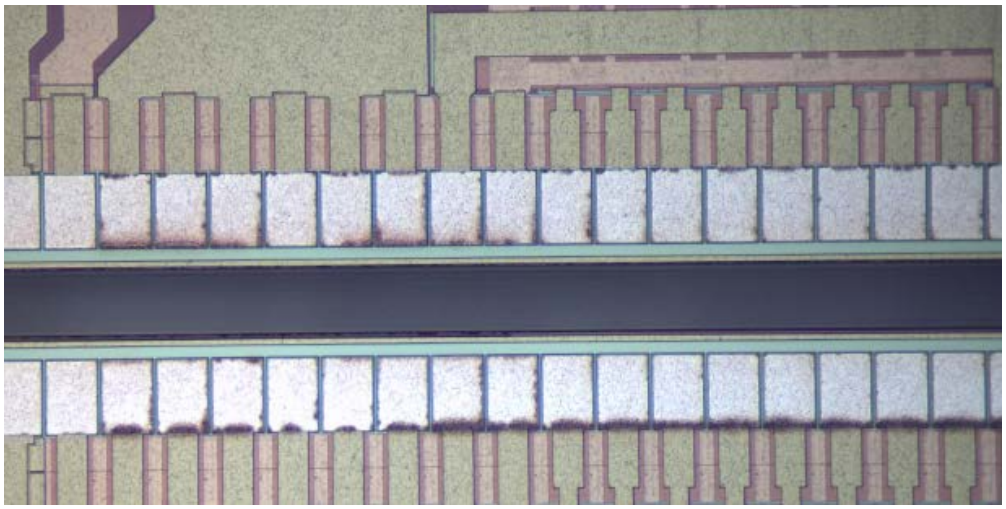


Figure 1.5: Heavy silicon dust reduced table speed and cut volume

Wire bond issues

Plastic packages typically will use gold ball bond process to connect the die to the package. The latest trend of using copper wire offers a significant cost saving while still following similar bonding construction as using gold wire.

Ball bond dimensions are smaller than the aluminum wedge bonds used in military and space hermetic assembly since the point of contact on the die is just the size of the ball, not the wedge.

Bond angles greater than 30° do not affect the adjacent bond even with tight bond pad spacing of 0.25 mils. With ball bonding, the wires exiting the ball from the top and will not touch the adjacent wire, a bond pad or bond.

This is not the case with wedge bonds as the bonds are typically longer due the structure of the bond. See Figure 2.1 below from MIL-STD-883 TM2010.

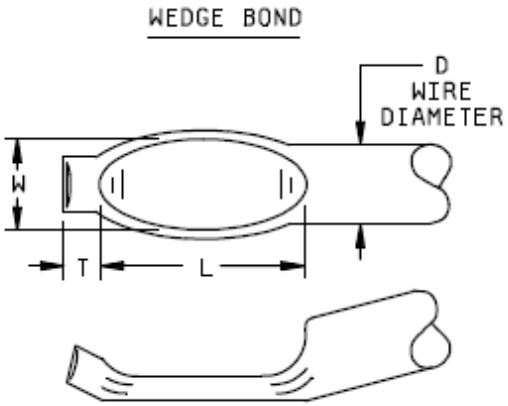


Fig. 2.1 from MIL-STD-883 TM2010

Due to the physical structure of the wedge bond, the bond angles play a critical role in connecting the die to the package. If the pad spacing is limited as it is with high pin count devices used in plastic packages, the heel or the bond tail can overlap the adjacent bond pad.

These structures are shown in Figures 2.2a and 2.2b on a high pin count LGA plastic package device being adapted for hermetic assembly. The gold ball bond process used for plastic assembly is not affected by bond angles or limited pad spacing.

Figure 2.2a. Ball bond

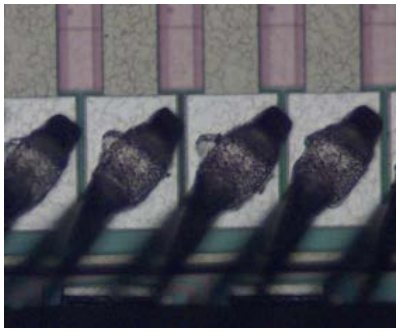


Figure 2.2b. Wedge bond

Wire Bond Process Change

Several ways exist to mitigate this problem and a combination of process changes may be required to achieve optimal assembly yield results.

The probability of device being redesigned at the die level for hermetic assembly only is very low due to the cost for low-volume production runs. This alternative is usually not an option.

Hermetic package layout redesign is an option to reduce the wire egress angle out to the package post. While this choice could be a costly proposition, it's considerably less expensive when compared to a die layout redesign and fabrication.

Other options include using smaller footprint wedges and changing the bond sequence from forward bond to reverse bond on connections with severe bond angles. This will eliminate the length of the bond tail thus reducing the overall bond length.

Wire crossover must be avoided on bonds located on the same tier since both the power and ground plane might be located on the same tier as the device input and/or output signal connections.

Other electrical considerations must be taken into account. Signal pairs where the impedance must be matched forces the length of these wire to be of similar dimension. The use of multiple tiers can also improve bond angle. The downside can be an increase in the package dimensions. Figure 2.3 is an excellent example using multiple tiers to maintain matching pair impedance while improving bond egress angles to as close to 90° and.

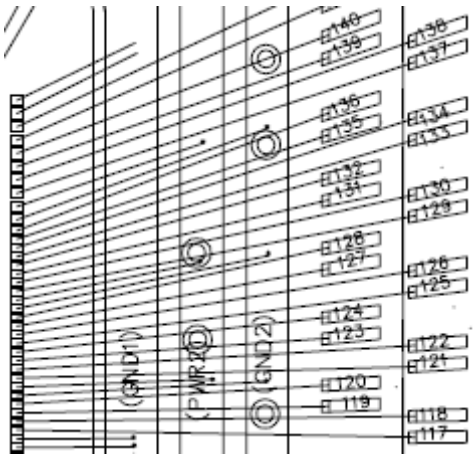


Figure 2.3 Multi-tier with match pairs

The methods discussed for wire bond make it possible to assemble a die (originally designed for a plastic package) in a hermetic package. A combination of these techniques often yields positive results, but there's no guarantee all devices will make this transition.

Package Seal Issues

Today's integrated circuit (IC) devices designed for plastic assembly may come with a die coat. The die coatings are added during the wafer fabrication process. This coating is typically used for additional protection of the circuitry from mechanical stresses caused by the plastic encapsulation process. Analog devices are particularly sensitive to these mechanical stresses which can alter the characteristics of the device.

The various die coat materials can be temperature sensitive and will peel off or blister at higher temperatures; typically greater than 300°C.

Hermetic packages have several methods of sealing which are all dependent on the package construction. Ceramic packages such as side brazed DIP (dual inline package) typically will use solder seal which has a eutectic liquidus state at about 280°C. CQFP (ceramic quad flat pack) may use a glass seal process with temperatures exceeding 400°C.

Since this die coat damage only occurs at the higher temperatures of the sealing process, it doesn't exist at the standard pre-cap inspection (MIL-STD-883 Test Method 2010 Internal Visual). This peeling or blistering of the die coat (as shown below in Figure 9) happens during sealing and will be rejectable per MIL-STD-883 Test Method 2013 Internal Visual For DPA (Destructive Physical Analysis).

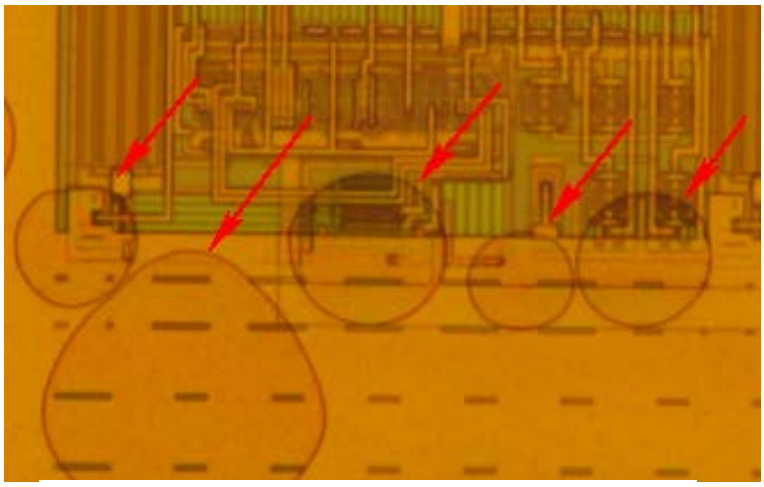
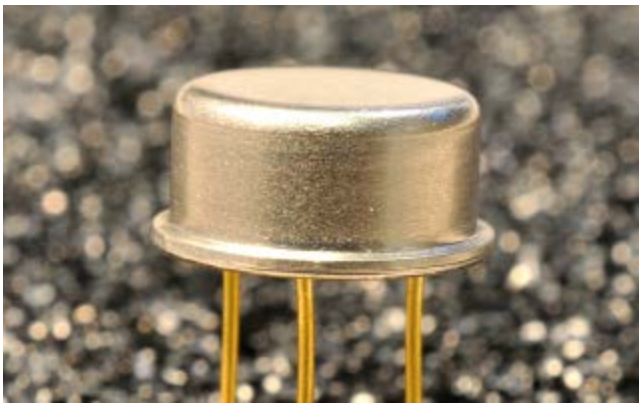


Figure 9: Die coat blistering cause by nominal sealing temperatures

One solution to the blister problem is the use of a weld seal process. This is the typical process used for sealing TO (transistor outline) header metal cans. During the process, the high welding temperatures are isolated to the seam area. For higher pin count devices, another seal process must be used. This process is called seam seal.



The seam seal process is normally used to create a seal between a metal lid and a metal package body. However, it can also be used to reflow a gold-tin preform between the metal lid and the ceramic package Kovar seal ring. This process also generates heat but it is localized and will not affect the die coat.

Figure 10: Standard Seam Sealing.

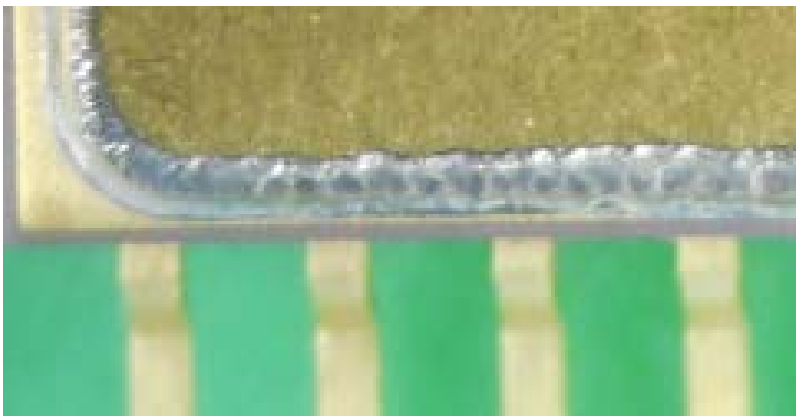


Figure 11: Seam Sealing using a solder preform.

Conclusion

The semiconductor market will continue to be driven by the commercial and industrial markets where die design considerations favor lower cost over long term reliability.

However, this doesn't mean the military and aerospace designs won't be able to benefit from the semiconductor processing breakthroughs happening today.

In this series, we covered ways Golden Altos uses to make this possible:

- Innovative wafer saw techniques for PCM removal
- Advanced packaging and wire bonding approaches
- Inventive sealing methods required when using coated die

Each device adaptation may have its own unique issues. Other assembly processes can be modified, as needed, to meet these challenges. Knowledgeable production operators working with experienced technical staff make these conversions a reality.

As a contract manufacturer, Golden Altos works with a wide range of wafers, dice, packaging configurations, and customer requirements. Each combination offers its own set of challenges. Our expertise in various wafer saw procedures, die attach techniques, wire bonding methods and package sealing approaches gives us the ability to deliver reliable, compliant product to our customers.